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EXAMINER	
YU, HENRY W	

ART UNIT	PAPER NUMBER
2182	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/613,897	BOESEL ET AL.	
	Examiner	Art Unit	
	HENRY YU	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6,7,9-15 and 17-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,7,9-15 and 17-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/23/2009, 08/17/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

INFORMATION CONCERNING RESPONSES

Response to Amendment

1. This Office Action is in response to applicant's communication filed on July 23, 2009, in response to PTO Office Action mailed on May 27, 2009. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, **claims 1, 9, 10, 13, 17-18, and 22** have been amended. **Claim 8** has been cancelled. As a result, **claims 1-4, 6-7, 9-15, and 17-22** are now pending in this application.

Response to Arguments

3. Applicant's arguments filed on March 30, 2009, in response to PTO Office Action mailed on July 23, 2009, have been fully considered. The arguments pertaining to the idea of processor disabling and reenabling are persuasive. Hence, the rejection has been withdrawn. However, upon further review a new ground of rejection has been made in view of Horigan et al. (Patent Number US 6,304,978 B1).

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1-4, 6-7, 9-15, 17, and 22** is rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram et al. (Publication Number US 2002/0176489 A1) in view of Tamura (Patent Number US 6,108,693) and Horigan et al. (Patent Number US 6,304,978 B1).

As per **claim 1**, Sriram et al. discloses "*a method of processing digital communication signals in a system including a processor and a plurality of buffers, the method comprising: buffering first digital samples corresponding to a first group of symbols into a first buffer and a second buffer* ***(two of the three buffers are available for processing by a correlator datapath (Page 1, paragraph 0009), with sections pointing to specific portions (e.g. PNi points to Chip i and PNi+1 points to Chip i+1); Figure 1)*** *at a sample rate* ***(represented by CCP iteration, which is a time duration; Page 3, paragraph 0040)****, wherein buffered first digital samples corresponding to earlier paths of the first group of symbols are stored in the first buffer, and buffered first digital samples corresponding to later paths of the first group of symbols are stored in the second buffer* ***(one of the two buffers of the triple data input buffer contains a plurality of early sets of chips while the remaining buffer contains a plurality of temporally late sets of chips (Page 1, paragraph 0009). As can be seen from Figure 1, the buffers are in sequential order)***."

Sriram et al. discloses "*processing, by the processor* ***(through a correlator datapath; Page 1, paragraph 0011)****, the first digital samples in the first buffer and the*

second buffer for all known paths of the first group of symbols during a first symbol group duration ***(despreading a plurality of triple data input buffer chips selected form the two buffers available for processing in a single correlation processing cycle; Page 1, paragraph 0011)***" and "*wherein the processor is clocked by a processor clock at a clock rate that is faster than and not synchronous with the sample rate* ***(as noted by the number of cycles for a particular CCP in conjunction with the existence of timing shifts (Page 3, paragraph 0041), the timing shifts indicating that the rate in general is not entirely synchronous)***."

Sriram et al. discloses "*simultaneously with processing the first digital samples, buffering second digital samples corresponding to a second group of symbols into the second buffer and a third buffer* ***(two of the three buffers are available for processing by a correlator datapath while (emphasis) the remaining buffer is being written into by incoming chips; Page 1, paragraph 0009)****, wherein buffered second digital samples corresponding to earlier paths of the second group of symbols are stored in the second buffer, and buffered second digital samples corresponding to later paths of the second group of symbols are stored in the third buffer* ***(one of the two buffers of the triple data input buffer contains a plurality of early sets of chips while the remaining buffer contains a plurality of temporally late sets of chips (Page 1, paragraph 0009). As can be seen from Figure 1, the buffers are in sequential order)***" and "*wherein the first symbol group duration represents a duration of time during which the second digital samples are buffered into the second buffer and the third buffer* ***(two of the three buffers are available for processing by a correlator***

datapath while (emphasis) the remaining buffer is being written into by incoming chips (Page 1, paragraph 0009). The use of the word 'while' indicates a same duration for processing and sample buffering)."

Sriram et al. discloses "*processing, by the processor* ***(through a correlator datapath; Page 1, paragraph 0011)****, the second digital samples in the second buffer and the third buffer for all known paths of the second group of symbols during the second symbol group duration* ***(despreading a plurality of triple data input buffer chips selected form the two buffers available for processing in a single correlation processing cycle; Page 1, paragraph 0011)***."

Sriram et al. discloses "*simultaneously with processing the second digital samples, buffering third digital samples corresponding to a third group of symbols into the third buffer and the first buffer* ***(two of the three buffers are available for processing by a correlator datapath while (emphasis) the remaining buffer is being written into by incoming chips; Page 1, paragraph 0009)****, wherein buffered third digital samples corresponding to earlier paths of the third group of symbols are stored in the third buffer, and buffered third digital samples corresponding to later paths of the third group of symbols are stored in the first buffer* ***(one of the two buffers of the triple data input buffer contains a plurality of early sets of chips while the remaining buffer contains a plurality of temporally late sets of chips (Page 1, paragraph 0009). As can be seen from Figure 1, the buffers are in sequential order)***" and "*wherein the second symbol group duration represents a duration of time during which the third digital samples are buffered into the third buffer and the first*

buffer ***(two of the three buffers are available for processing by a correlator datapath while (emphasis) the remaining buffer is being written into by incoming chips (Page 1, paragraph 0009). The use of the word 'while' indicates a same duration for processing and sample buffering)***."

Sriram et al. discloses "*processing the third digital samples in the third buffer and the first buffer for all known paths of the third group of symbols during the third symbol group duration* ***(despreading a plurality of triple data input buffer chips selected form the two buffers available for processing in a single correlation processing cycle; Page 1, paragraph 0011)***."

Tamura discloses the idea of processor/component disabling upon the completion of a task or process, as disclosed in the limitations "*disabling the processor upon completion of processing the first digital samples* ***(there exists a status flag for controlling write and read enable/disable of the communication buffer, where the initial state of the status flag is write-enabled and read-disabled. It is noted that upon write completion the status flag is set from read-disabled to read-enabled, and upon read completion the status flag is set from write-disabled to write-enabled (Column 2, lines 56-67). This is interpreted as write being disabled by a write completion notification, with the write processing not set to enabled until the read process is completed)*** *...through a remainder of the first symbol group duration* ***(the wording of this limitation indicates that disabling occurs after completion as a result of processing during the remainder duration of the symbol group)***," "*disabling the processor upon completion of processing the second digital*

samples ***(Column 2, lines 56-67)****...through a remainder of the second symbol group duration* ***(the wording of this limitation indicates that disabling occurs after completion as a result of processing during the remainder duration of the symbol group)***," and "*disabling the processor upon completion of processing the third digital samples* ***(Column 2, lines 56-67)****…through a remainder of the third symbol group duration* ***(the wording of this limitation indicates that disabling occurs after completion as a result of processing during the remainder duration of the symbol group)***."

Horigan et al. discloses the idea of clock gating where an idle processor is disabled as disclosed in the limitation "*by gating off the processor clock, wherein the processor remains disabled* ***(Column 1, lines 40-43)***" and the idea of enabling a processor again when needed as disclosed in the limitation "*at a beginning of a second symbol group duration that occurs consecutively with an end of the first symbol group duration, enabling the processor to process the second digital samples* ***(clocks are again enabled when the disabled portion of the component is needed; Column 1, lines 43-46)***," which also applies to the limitation "*at a beginning of a third symbol group duration that occurs consecutively with an end of the second symbol group duration, enabling the processor to process the third digital samples* ***(clocks are again enabled when the disabled portion of the component is needed; Column 1, lines 43-46)***."

Sriram et al., Tamura, and Horigan et al. are analogous art in that they are from the same field of communication systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the elements of Sriram et al. with the idea of idea of processor/component disabling upon the completion of a task or process as disclosed by Tamura, which notes instances of data being inaccessible if a particular process is still active **[Column 1, lines 51-58]**. Hence, it would be obvious for one skilled in the art to disable a processor once a task has been completed in order to allow further processing to occur.

As for Horigan et al., clock gating allows for the saving of power without impacting performance **[Column 1, lines 43-45]**.

As per **claim 2**, the combination of Sriram et al., Tamura, and Horigan et al. discloses "*the method*" (*see rejection to* ***claim 1*** *above*). Sriram et al. further discloses "*the plurality of buffers hold a number of digital samples* ***(despread symbols dumped into a finger symbol buffer)****, the number being adjusted for communication conditions* ***(number of despread symbols dumped into a finger symbol buffer depends on the value of SF (symbol fingers); Page 3, paragraph 0041)***."

As per **claim 3**, the combination of Sriram et al., Tamura, and Horigan et al. discloses "*the method*" (*see rejection to* ***claim 1*** *above*). Sriram et al. further discloses "*the communication conditions include a communication technology* ***(system/method capable of supporting spread-spectrum CDMA; Page 4, paragraph 0048)*** *and anticipated maximum useful multi-path delay in an environment* ***(system/method is capable of handling special cases of early/ontime/late correlations that occur***

when the on-time sample is near a chip boundary; Page 4, paragraph 0044; FIG. 4a-4c)."

As per **claim 4**, the combination of Sriram et al., Tamura, and Horigan et al. discloses "*the method*" (*see rejection to* ***claim 1*** *above*). Sriram et al. further discloses "*received information relevant to a given group of transmitted symbols* ***(input buffer chips)*** *is processed in one iteration, without a need to store intermediate results for the given group of transmitted symbols* ***(despreading a plurality of triple data input buffer chips by the correlator datapath in a single processing cycle; Page 1, paragraph 0011)***."

As per **claim 6**, the combination of Sriram et al., Tamura, and Horigan et al. discloses "*the method*" (*see rejection to* ***claim 1*** *above*). Sriram et al. further discloses "*tuning a receiver to a first channel, storing received symbols from the first channel* ***(receiving chip samples into the triple data input buffer (Page 1, paragraph 0010) with an input buffer associated with time tracking of a particular symbol multipath; Page 1, paragraph 0007)****, and tuning the receiver to a second channel* ***(timing change associated with the chip samples, indicating that samples at another timing value has been inputted beforehand; Page 1, paragraph 0012)***."

As per **claim 7**, the combination of Sriram et al., Tamura, and Horigan et al. discloses "*the method*" (*see rejection to* ***claim 1*** *above*). Sriram et al. further discloses "*processing symbols received from the first channel during extra cycles of processing while the receiver is tuned to the second channel* ***(in special cases when a timing change request has arrived, one extra cycle is idled to adjust for the time change***

before the system resumes normal operation (Page 1, paragraph 0007; Page 3, paragraph 0041). Furthermore, two of the three buffers are avaliable for processing by a correlator datapath while (emphasis) the remaining buffer is being writtten into by incoming chips (Page 1, paragraph 0009), indicating receiver focus elsewhere during the processing of the first set of symbols)."

As per **claim 9**, Sriram et al. discloses "*a method of processing digital communication signals in a system including a plurality of buffers, the method comprising: processing, by a processor* ***(through a correlator datapath; Page 1, paragraph 0011)*** *during a first symbol group duration* ***(despreading a plurality of triple data input buffer chips selected form the two buffers available for processing in a single correlation processing cycle; Page 1, paragraph 0011)****, symbols corresponding to a first group of symbols to be processed and from all known paths* ***(time tracking that allows demodulation of a particular multipath at a particular timing condition; Page 2, paragraph 0026)****, wherein the first group of symbols in a first path start in a first buffer and end in a second buffer* ***(two of the three buffers are available for processing by a correlator datapath (Page 1, paragraph 0009), with sections pointing to specific portions (e.g. PNi points to Chip i and PNi+1 points to Chip i+1); Figure 1)****, and receiving samples at a third buffer simultaneously with processing the first group of symbols* ***(two of the three buffers are available for processing by a correlator datapath while (emphasis) the remaining buffer is being written into by incoming chips; Page 1, paragraph 0009)***."

Sriram et al. discloses "*processing, by the processor* ***(through a correlator datapath; Page 1, paragraph 0011)*** *during a second symbol group duration, symbols corresponding to a second group of symbols to be processed and from all known paths, wherein the second group of symbols in a second path start in the second buffer and end in the third buffer* ***(two of the three buffers are available for processing by a correlator datapath (Page 1, paragraph 0009), with sections pointing to specific portions (e.g. PNi points to Chip i and PNi+1 points to Chip i+1); Figure 1)****, and receiving samples at the first buffer simultaneously with processing the second group of symbols* ***(two of the three buffers are available for processing by a correlator datapath while (emphasis) the remaining buffer is being written into by incoming chips; Page 1, paragraph 0009)***."

Sriram et al. discloses "*processing, by the processor* ***(through a correlator datapath; Page 1, paragraph 0011)*** *during a third symbol group duration, symbols corresponding to a third group of symbols to be processed and from all known paths, wherein the third group of symbols in a third path start in the third buffer and end in the first buffer* ***(two of the three buffers are available for processing by a correlator datapath (Page 1, paragraph 0009), with sections pointing to specific portions (e.g. PNi points to Chip i and PNi+1 points to Chip i+1); Figure 1)****, and receiving samples at the second buffer while the third group of symbols is being processed* ***(two of the three buffers are available for processing by a correlator datapath while (emphasis) the remaining buffer is being written into by incoming chips; Page 1, paragraph 0009)***," and "*receiving samples at the second buffer simultaneously with*

processing the third group of symbols ***(two of the three buffers are available for processing by a correlator datapath while (emphasis) the remaining buffer is being written into by incoming chips; Page 1, paragraph 0009)***."

Sriram et al. discloses "*adapting duration time of the processing of the first, second, and third groups based on channel and signal conditions* ***(number of despread symbols dumped into a finger symbol buffer depends on the value of SF (symbol fingers); Page 3, paragraph 0041)***."

Tamura discloses the idea of processor/component disabling upon the completion of a task or process, as disclosed in the limitations "*disabling the processor upon completion of processing the symbols corresponding to the first group* ***(there exists a status flag for controlling write and read enable/disable of the communication buffer, where the initial state of the status flag is write-enabled and read-disabled. It is noted that upon write completion the status flag is set from read-disabled to read-enabled, and upon read completion the status flag is set from write-disabled to write-enabled (Column 2, lines 56-67). This is interpreted as write being disabled by a write completion notification, with the write processing not set to enabled until the read process is completed)****…through a remainder of the first symbol group duration* ***(the wording of this limitation indicates that disabling occurs after completion as a result of processing during the remainder duration of the symbol group)****, wherein the first symbol group duration ends when samples in the third buffer are ready for processing* ***(interpretation where write is disabled by a write completion notification, with the write processing not***

set to enabled until the read process is completed, also applies here)," "*disabling the processor upon completion of processing the symbols corresponding to the second group* ***(Column 2, lines 56-67)*** *…through a remainder of the second symbol group duration* ***(the wording of this limitation indicates that disabling occurs after completion as a result of processing during the remainder duration of the symbol group)****, wherein the second symbol group duration ends when samples in the first buffer are ready for processing* ***(interpretation where write is disabled by a write completion notification, with the write processing not set to enabled until the read process is completed, also applies here)***," and "*disabling the processor upon completion of processing the symbols corresponding to the third group* ***(Column 2, lines 56-67)****…through a remainder of the third symbol group duration, wherein the third symbol group duration ends when samples in the second buffer are ready for processing* ***(interpretation where write is disabled by a write completion notification, with the write processing not set to enabled until the read process is completed, also applies here)***."

Horigan et al. discloses the idea of clock gating where an idle processor is disabled as disclosed in the limitation "*by gating off the processor clock, wherein the processor remains disabled* ***(Column 1, lines 40-43)***."

Sriram et al., Tamura, and Horigan et al. are analogous art in that they are from the same field of communication systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the elements of Sriram et al. with the idea of idea of

processor/component disabling upon the completion of a task or process as disclosed by Tamura, which notes instances of data being inaccessible if a particular process is still active **[Column 1, lines 51-58]**. Hence, it would be obvious for one skilled in the art to disable a processor once a task has been completed in order to allow further processing to occur.

As for Horigan et al., clock gating allows for the saving of power without impacting performance **[Column 1, lines 43-45]**.

As per **claim 10**, Sriram et al. discloses "*an apparatus to process digital communication signals, the apparatus comprising: a plurality of buffers* ***(triple data buffer; Page 1, paragraph 0009)***," "*a processing unit* ***(correlator coprocessor; Figure 7)***," "*programmed memory having instructions* ***(configuration tables; Figure 7)*** *directing the processing unit* ***(correlator coprocessor through a controller)*** *to process first digital samples corresponding to a first group of symbols to be processed in a plurality of buffers, the first digital samples starting in a first buffer of the plurality of buffers and ending in a second buffer of the plurality of buffers* ***(two of the three buffers are available for processing by a correlator datapath (Page 1, paragraph 0009), with sections pointing to specific portions (e.g. PNi points to Chip i and PNi+1 points to Chip i+1); Figure 1)***," and "*wherein the processing unit processes the first digital samples during a first symbol group duration* ***(despreading a plurality of triple data input buffer chips selected form the two buffers available for processing in a single correlation processing cycle; Page 1, paragraph 0011)****, and wherein additional digital samples are received at a third buffer of the plurality of buffers*

simultaneously with the first digital samples being processed ***(two of the three buffers are available for processing by a correlator datapath while (emphasis) the remaining buffer is being written into by incoming chips; Page 1, paragraph 0009)***."

Tamura discloses the idea of processor/component disabling upon the completion of a task or process, as disclosed in the limitations "*wherein, prior to an end of the first symbol group duration, the processing unit is disabled upon completion of processing the first digital samples* ***(there exists a status flag for controlling write and read enable/disable of the communication buffer, where the initial state of the status flag is write-enabled and read-disabled. It is noted that upon write completion the status flag is set from read-disabled to read-enabled, and upon read completion the status flag is set from write-disabled to write-enabled (Column 2, lines 56-67). This is interpreted as write being disabled by a write completion notification, with the write processing not set to enabled until the read process is completed)****…through a remainder of the first symbol group duration* ***(the wording of this limitation indicates that disabling occurs after completion as a result of processing during the remainder duration of the symbol group)***."

Tamura also discloses "*wherein the first symbol group duration represents a duration of time that ends upon completion of synchronously filling the third buffer with the additional digital samples* ***(interpretation where write is disabled by a write completion notification, with the write processing not set to enabled until the read process is completed, also applies here; Column 2, lines 56-67)***."

Horigan et al. discloses the idea of clock gating where an idle processor is disabled as disclosed in the limitation "*by gating off the processor clock, wherein the processor remains disabled* ***(Column 1, lines 40-43)***."

Sriram et al., Tamura, and Horigan et al. are analogous art in that they are from the same field of communication systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the elements of Sriram et al. with the idea of idea of processor/component disabling upon the completion of a task or process as disclosed by Tamura, which notes instances of data being inaccessible if a particular process is still active **[Column 1, lines 51-58]**. Hence, it would be obvious for one skilled in the art to disable a processor once a task has been completed in order to allow further processing to occur.

As for Horigan et al., clock gating allows for the saving of power without impacting performance **[Column 1, lines 43-45]**.

As per **claim 11**, the combination of Sriram et al., Tamura, and Horigan et al. discloses "*the apparatus*" (*see rejection to* ***claim 10*** *above*). Sriram et al. further discloses "*comprising input and output busses* ***(data path; Figure 7)*** *operable to permit random access to the plurality of buffers during processing* ***(demodulation even when the mulipath is not constant; Page 2, paragraph 0026)***."

As per **claim 12**, the combination of Sriram et al., Tamura, and Horigan et al. discloses "*the apparatus*" (*see rejection to* ***claim 10*** *above*). Sriram et al. further

discloses "*symbols are processed in a different group of buffers after a process iteration is complete* ***(at each iteration, the buffer is shifted over by 16 chips; Figure 1)***."

As per **claim 13**, Sriram et al. discloses "*a method of processing digital communication signals, the method comprising: receiving a communication signal at a receiver* ***(date from Rx source into input buffers; Figure 7)***" and "*communicating digital samples from the received communication signal into a first group of sample buffers* ***(signals from Rx source 0 and 1 to input buffers; Figure 7)****, wherein the digital samples include first symbols* ***(symbol despreading; Page 2, paragraph 0033)***."

Sriram et al. discloses "*processing, by a processor during a first symbol group duration, the first symbols in the first group of sample buffers* ***(two of the three buffers, consisting of one group, are processed by a correlator datapath (Page 1, paragraph 0009), with sections pointing to specific portions (e.g. PNi points to Chip i and PNi+1 points to Chip i+1); Figure 1)*** *while simultaneously communicating additional digital samples from the receiver into a second group of sample buffers during the processing* ***(remaining buffer, for the second group, is being written into by incoming chips; Page 1, paragraph 0009)***."

Tamura discloses the idea of processor/component disabling upon the completion of a task or process, as disclosed in the limitations "*prior to an end of the first symbol group duration, disabling the processor upon completion of processing the first symbols in the first group of sample buffers* ***(there exists a status flag for controlling write and read enable/disable of the communication buffer, where the initial state of the status flag is write-enabled and read-disabled. It is noted that***

upon write completion the status flag is set from read-disabled to read-enabled, and upon read completion the status flag is set from write-disabled to write-enabled (Column 2, lines 56-67). This is interpreted as write being disabled by a write completion notification, with the write processing not set to enabled until the read process is completed)*…through a remainder of the first symbol group duration* ***(the wording of this limitation indicates that disabling occurs after completion as a result of processing during the remainder duration of the symbol group)***" and "*at a beginning of a second symbol group duration, enabling the processor to process the second symbols in the second group of sample buffers during the second symbol group duration* ***(there exists a status flag for controlling write and read enable/disable of the communication buffer, where the initial state of the status flag is write-enabled and read-disabled. It is noted that upon write completion the status flag is set from read-disabled to read-enabled, and upon read completion the status flag is set from write-disabled to write-enabled; Column 2, lines 56-67)****, wherein the beginning of the second symbol group duration occurs consecutively with the end of the first symbol group duration* ***(interpretation where write is disabled by a write completion notification, with the write processing not set to enabled until the read process is completed, also applies here)***."

Tamura also discloses "*wherein the additional digital samples include second symbols, and wherein the first symbol group duration represents a duration of time during which the second group of sample buffers is filled with the additional digital samples* ***(interpretation where write is disabled by a write completion notification,***

with the write processing not set to enabled until the read process is completed, also applies here; Column 2, lines 56-67)."

Horigan et al. discloses the idea of clock gating where an idle processor is disabled as disclosed in the limitation "*by gating off the processor clock, wherein the processor remains disabled* ***(Column 1, lines 40-43)***."

Sriram et al., Tamura, and Horigan et al. are analogous art in that they are from the same field of communication systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the elements of Sriram et al. with the idea of idea of processor/component disabling upon the completion of a task or process as disclosed by Tamura, which notes instances of data being inaccessible if a particular process is still active **[Column 1, lines 51-58]**. Hence, it would be obvious for one skilled in the art to disable a processor once a task has been completed in order to allow further processing to occur.

As for Horigan et al., clock gating allows for the saving of power without impacting performance **[Column 1, lines 43-45]**.

As per **claim 14**, the combination of Sriram et al., Tamura, and Horigan et al. discloses "*the method apparatus*" (*see rejection to* ***claim 13*** *above*). Sriram et al. further discloses "*after symbols in a symbol path are completely processed, designating sample buffers in the first group of sample buffers as being in the second group of sample buffers* ***(after the first iteration, there is a shift to the right of 16 chips, where the second group of 16 chips become part of the group of buffers***

accessible for processing in the next iteration k+1; Figure 1)" and "*designating sample buffers in the second group of sample buffers as being in the first group of sample buffers, whereby sample buffers are rotated between processing iterations and digital sample receiving operations* ***(the buffer is circular (Page 1, paragraph 0007) and at each iteration the buffer 'slides' by an interval of 16 chips (each buffer consists of 16 chips) in a circular manner; Page 3, paragraph 0040; Figure 2)***."

As per **claim 15**, the combination of Sriram et al., Tamura, and Horigan et al. discloses "*the method apparatus*" (*see rejection to* ***claim 13*** *above*). Sriram et al. further discloses "*sample buffers in the first group of sample buffers designated as being in the second group of sample buffers include all the sample buffers in the first group of sample buffers* ***(after the first iteration, there is a shift to the right of 16 chips, where the second group of 16 chips become part of the group of buffers accessible for processing in the next iteration k+1; Figure 1)*** *except a sample buffer having an end of a symbol path* ***(at iteration k+1, buffers from the first iteration k that include the notation 'x' for 'on-time sample being used for despread' are not included; Figure 1)***."

As per **claim 17**, Sriram et al. discloses "*a method of processing digital communication signals in a system including a processor and a plurality of buffers, the method comprising: processing, by the processor during a first symbol group duration, first samples corresponding to a first group of symbols to be processed, wherein the first samples start in a first buffer and end in a second buffer* ***(two of the three buffers are available for processing by a correlator datapath (Page 1, paragraph 0009), with***

sections pointing to specific portions (e.g. PNi points to Chip i and PNi+1 points to Chip i+1); Figure 1)*, and simultaneously receiving second samples at a third buffer during the processing of the first group of symbols* ***(remaining buffer is being written into by incoming chips; Page 1, paragraph 0009)***," where the buffer is circular **(Page 1, paragraph 0007)** and at each iteration the buffer "slides" by an interval of 16 chips (with each buffer consisting of 16 chips) in a circular manner to enable the datapath to have access to another buffer **(Page 3, paragraph 0040; Figure 2)**.

Since the triple buffer of the system/method is circular, Sriram et al. also discloses "*processing, by the processor during a second symbol group duration, the second samples corresponding to the second group of symbols to be processed, wherein the second samples start in the second buffer and end in the third buffer* ***(two of the three buffers are available for processing by a correlator datapath (Page 1, paragraph 0009), with sections pointing to specific portions (e.g. PNi points to Chip i and PNi+1 points to Chip i+1); Figure 1)****, and simultaneously receiving third samples at the first buffer during the processing of the second group of symbols* ***(two of the three buffers are available for processing by a correlator datapath while (emphasis) the remaining buffer is being written into by incoming chips; Page 1, paragraph 0009)***."

Sriram et al. discloses "*processing, by the processor during a third symbol group duration, the third samples corresponding to the third group of symbols to be processed, wherein the third samples start in the third buffer and end in the first buffer* ***(two of the three buffers are available for processing by a correlator datapath (Page 1,***

paragraph 0009), with sections pointing to specific portions (e.g. PNi points to Chip i and PNi+1 points to Chip i+1); Figure 1)*, and simultaneously receiving fourth samples at the second buffer while during the processing of the third group of symbols* ***(two of the three buffers are available for processing by a correlator datapath while (emphasis) the remaining buffer is being written into by incoming chips; Page 1, paragraph 0009)***."

Tamura discloses the idea of processor/component disabling upon the completion of a task or process, as disclosed in the limitations "*prior to an end of the first symbol group duration, disabling the processor upon completion of processing the first samples corresponding to the first group* ***(there exists a status flag for controlling write and read enable/disable of the communication buffer, where the initial state of the status flag is write-enabled and read-disabled. It is noted that upon write completion the status flag is set from read-disabled to read-enabled, and upon read completion the status flag is set from write-disabled to write-enabled; Column 2, lines 56-67)****...during a remainder of the first symbol group duration* ***(the wording of this limitation indicates that disabling occurs after completion as a result of processing during the remainder duration of the symbol group)***," "*prior to an end of the second symbol group duration, disabling the processor upon completion of processing the symbols corresponding to the second group* ***(Column 2, lines 56-67)****…during a remainder of the second symbol group duration* ***(the wording of this limitation indicates that disabling occurs after completion as a result of processing during the remainder duration of the symbol group)***," and

"*prior to an end of the third symbol group duration, disabling the processor upon completion of processing the symbols corresponding to the third group* ***(Column 2, lines 56-67)****…during a remainder of the third symbol group duration* ***(the wording of this limitation indicates that disabling occurs after completion as a result of processing during the remainder duration of the symbol group)***."

Tamura also discloses "*wherein the second samples correspond to a second group of symbols to be processed, and the first symbol group duration represents a duration of time that ends upon completion of synchronously filling the third buffer with the second samples* ***(interpretation where write is disabled by a write completion notification, with the write processing not set to enabled until the read process is completed, also applies here; Column 2, lines 56-67)***," "*wherein the third samples correspond to a third group of symbols to be processed, and the second symbol group duration represents a duration of time that ends upon completion of synchronously filling the first buffer with the third samples* ***(interpretation where write is disabled by a write completion notification, with the write processing not set to enabled until the read process is completed, also applies here; Column 2, lines 56-67)***," and "*wherein the fourth samples correspond to a fourth group of symbols to be processed, and the third symbol group duration represents a duration of time that ends upon completion of synchronously filling the second buffer with the fourth samples* ***(interpretation where write is disabled by a write completion notification, with the write processing not set to enabled until the read process is completed, also applies here; Column 2, lines 56-67)***."

Horigan et al. discloses the idea of clock gating where an idle processor is disabled as disclosed in the limitation "*by gating off the processor clock, wherein the processor remains disabled* ***(Column 1, lines 40-43)***."

Sriram et al., Tamura, and Horigan et al. are analogous art in that they are from the same field of communication systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the elements of Sriram et al. with the idea of idea of processor/component disabling upon the completion of a task or process as disclosed by Tamura, which notes instances of data being inaccessible if a particular process is still active **[Column 1, lines 51-58]**. Hence, it would be obvious for one skilled in the art to disable a processor once a task has been completed in order to allow further processing to occur.

As for Horigan et al., clock gating allows for the saving of power without impacting performance **[Column 1, lines 43-45]**.

As per **claim 22**, Sriram et al. discloses "*an apparatus to process digital communication signals, the apparatus comprising: a plurality of buffers****(triple data buffer; Page 1, paragraph 0009)***," "*a processing unit* ***(correlator coprocessor; Figure 7)***," and "*programmed memory having instructions* ***(configuration tables; Figure 7)*** *directing the processing unit* ***(correlator coprocessor through a controller)*** *to process first digital samples corresponding to a group of symbols to be processed in a plurality of buffers, the first digital samples starting in a first buffer of the plurality of buffers and ending in a second buffer of the plurality of buffers* ***(two of the three***

buffers are available for processing by a correlator datapath (Page 1, paragraph 0009), with sections pointing to specific portions (e.g. PNi points to Chip i and PNi+1 points to Chip i+1); Figure 1)."

Sriram et al. discloses "*wherein the processing unit* ***(through a correlator datapath)*** *processes the first digital samples during a first symbol group duration* ***(despreading a plurality of triple data input buffer chips selected form the two buffers available for processing in a single correlation processing cycle; Page 1, paragraph 0011)****, and wherein additional digital samples are received at a third buffer of the plurality of buffers simultaneously with the first digital samples being processed* ***(two of the three buffers are available for processing by a correlator datapath while (emphasis) the remaining buffer is being written into by incoming chips; Page 1, paragraph 0009)****, and wherein the processing unit is operable to select digital samples or an intermediate result from a buffer coupled to the processing unit* ***(despreading a plurality of triple data input buffer chips selected from two buffers available for processing; Page 1, paragraph 0011)***."

Tamura discloses the idea of processor/component disabling upon the completion of a task or process, as disclosed in the limitations "*wherein, prior to an end of the first symbol group duration, the processing unit is disabled upon completion of processing the first digital samples* ***(there exists a status flag for controlling write and read enable/disable of the communication buffer, where the initial state of the status flag is write-enabled and read-disabled. It is noted that upon write completion the status flag is set from read-disabled to read-enabled, and upon***

read completion the status flag is set from write-disabled to write-enabled (Column 2, lines 56-67). This is interpreted as write being disabled by a write completion notification, with the write processing not set to enabled until the read process is completed) *…through a remainder of the first symbol group duration* ***(the wording of this limitation indicates that disabling occurs after completion as a result of processing during the remainder duration of the symbol group)****, and wherein the processor is enabled at a beginning of a second symbol group duration, wherein the end of the first symbol group duration coincides with the beginning of the second symbol group duration* ***(interpretation where write is disabled by a write completion notification, with the write processing not set to enabled until the read process is completed, also applies here)****.*"

Horigan et al. discloses the idea of clock gating where an idle processor is disabled as disclosed in the limitation "*by gating off the processor clock, wherein the processor remains disabled* ***(Column 1, lines 40-43)***."

Sriram et al., Tamura, and Horigan et al. are analogous art in that they are from the same field of communication systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the elements of Sriram et al. with the idea of idea of processor/component disabling upon the completion of a task or process as disclosed by Tamura, which notes instances of data being inaccessible if a particular process is still active **[Column 1, lines 51-58]**. Hence, it would be obvious for one skilled in the art

to disable a processor once a task has been completed in order to allow further processing to occur.

As for Horigan et al., clock gating allows for the saving of power without impacting performance **[Column 1, lines 43-45]**.

6. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram et al. (Publication Number US 2002/0176489 A1) and Tamura (Patent Number US 6,108,693) and Horigan et al. (Patent Number US 6,304,978 B1), in view of Lee et al. (Patent Number US 6,650,140 B2).

As per **claim 5**, the combination of Sriram et al., Tamura, and Horigan et al. discloses "*the method*" (*see rejection to* ***claim 1*** *above*). Though Sriam et al. discloses "*process received symbols in the plurality of buffers* ***(despreading a plurality of triple data input buffer chips selected from two buffers; Page 1, paragraph 0011)***," the combination of Sriram et al. and Tamura does not disclose "*turning off a receiver subsystem and continuing to process received symbols in the plurality of buffers*."

Lee et al. discloses "*turning off a receiver subsystem and continuing to process received symbols in the plurality of buffers* ***(receiver can be turned off if it is not needed; Column 15, lines 40-44)***."

Sriram et al., Tamura, Horigan et al., and Lee et al. are analogous art in that they are from the same field of communication systems and interfacing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the method as disclosed by the combination of Sriram et al., Tamura, and Horigan et al. with the idea of the turning off the receiver as disclosed by

Lee et al., which Lee et al. notes is related to a power-down mode **(Column 15, lines 40-41)**. The ability to power down any unused components can allow a device to save power, especially in mobile devices that run off a battery with a finite amount of power.

7. **Claim 16** is rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram et al. (Publication Number US 2002/0176489 A1), Tamura (Patent Number US 6,108,693), and Horigan et al. (Patent Number US 6,304,978 B1) in view of Roohparvar (Patent Number US 6,615,307 B1).

As per **claim 16**, the combination of Sriram et al., Tamura, and Horigan et al. discloses "*the method*" (*see rejection to* ***claim 13*** *above*). However, the combination of Sriram et al., Tamura, and Horigan et al. does not disclose "*shutting down sample buffers when sufficient processing is complete*."

Roohparvar "*shutting down sample buffers* ***(input buffers)*** *when sufficient processing is complete* ***(during power-down modes, which shows that there are no further processes to handle; Column 5, lines 6-8)***."

Sriram et al., Tamura, Horigan et al., and Roohparvar are analogous art in that they are from the same field of interface buffering.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the method of processing digital communication signals in a system including a plurality of buffers as disclosed by the combination of Sriram et al., Tamura, and Horigan et al. with the idea of the turning off the buffers as disclosed by Roohparvar, which Roohparvar notes is related to providing low standby power **(Column 5, lines 6-8)**. The ability to power down any unused components can allow a

device to save power, especially in mobile devices that run off a battery with a finite amount of power.

8. **Claims 18-21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram et al. (Publication Number US 2002/0176489 A1) in view of Tamura (Patent Number US 6,108,693), Horigan et al. (Patent Number US 6,304,978 B1), and Robertson et al. (Publication Number US 2001/0038633 A1).

As per **claim 18**, Sriram et al. discloses "*a method of processing digital communication signals in a system including a processor and a plurality of buffers, the method comprising: processing, by the processor during a first symbol group duration, from all known paths of a first group of symbols* ***(time tracking that allows demodulation of a particular multipath at a particular timing condition; Page 2, paragraph 0026)****, wherein buffered digital samples corresponding to the first group of symbols start in a first buffer and end in a third buffer* ***(two of the three buffers are available for processing by a correlator datapath while the remaining buffer is being written into by incoming chips; Page 1, paragraph 0009)****, and receiving samples at a fourth buffer and a fifth buffer simultaneously with the first group of symbols being processed* ***(two of the three buffers are available for processing by a correlator datapath while (emphasis) the remaining buffer is being written into by incoming chips; Page 1, paragraph 0009)***," where the buffer is circular **(Page 1, paragraph 0007)** and at each iteration the buffer "slides" by an interval of 16 chips (with each buffer consisting of 16 chips) in a circular manner to enable the datapath to have access to another buffer **(Page 3, paragraph 0040; Figure 2)**.

Sriram et al. also discloses the idea of processing from one set of buffers while writing into another set of buffers as disclosed in "*receiving samples at the first buffer and second buffer simultaneously with the second group of symbols being processed* ***(two of the three buffers are available for processing by a correlator datapath while (emphasis) the remaining buffer is being written into by incoming chips; Page 1, paragraph 0009)***," "*receiving samples at the fourth buffer and the third buffer simultaneously with the third group of symbols being processed* ***(two of the three buffers are available for processing by a correlator datapath while (emphasis) the remaining buffer is being written into by incoming chips; Page 1, paragraph 0009)***," "*receiving samples at a second buffer and the fifth buffer simultaneously with the fourth group of symbols being processed* ***(two of the three buffers are available for processing by a correlator datapath while (emphasis) the remaining buffer is being written into by incoming chips; Page 1, paragraph 0009)***," "*receiving samples at the fourth buffer and the first buffer simultaneously with the fifth group of symbols being processed* ***(two of the three buffers are available for processing by a correlator datapath while (emphasis) the remaining buffer is being written into by incoming chips; Page 1, paragraph 0009)***," and "*receiving samples at the second buffer and the first buffer simultaneously with the sixth group of symbols being processed* ***(two of the three buffers are available for processing by a correlator datapath while (emphasis) the remaining buffer is being written into by incoming chips; Page 1, paragraph 0009)***."

Concerning the use of five buffers, Robertson et al. discloses "*processing, by the processor during the second symbol group duration, from all known paths of a second group of symbols, wherein buffered digital samples corresponding to the second group of symbols start in the third buffer and end in the fifth buffer* ***(several of the buffers are available for processing by a correlator datapath and remaining buffer is written into by incoming chips; Page 1, paragraph 0009)***," "*processing, by the processor during the third symbol group duration, from all known paths of a third group of symbols, wherein buffered digital samples corresponding to the third group of symbols start in the fifth buffer and end in the first buffer* ***(several of the buffers are available for processing by a correlator datapath and remaining buffer is written into by incoming chips; Page 1, paragraph 0009)***," "*processing, by the processor during the fourth symbol group duration, from all known paths of a fourth group of symbols, wherein buffered digital samples corresponding to the fourth group of symbols start in the first buffer and end in the third buffer* ***(several of the buffers are available for processing by a correlator datapath and remaining buffer is written into by incoming chips; Page 1, paragraph 0009)***," "*processing, by the processor during the fifth symbol group duration, from all known paths of a fifth group of symbols, wherein buffered digital samples corresponding to the fifth group of symbols start in the third buffer and end in the fifth buffer* ***(several of the buffers are available for processing by a correlator datapath and remaining buffer is written into by incoming chips; Page 1, paragraph 0009)***," and "*processing, by the processor during the sixth symbol group duration, from all known paths of a sixth group of symbols, wherein buffered*

digital samples corresponding to the sixth group of symbols start in the fifth buffer and end in the first buffer ***(several of the buffers are available for processing by a correlator datapath and remaining buffer is written into by incoming chips; Page 1, paragraph 0009)***."

Tamura discloses the idea of processor/component disabling upon the completion of a task or process, as disclosed in the limitations "*prior to an end of the first symbol group duration, disabling the processor upon completion of processing the first group of symbols by…during a remainder of the first symbol group duration* ***(there exists a status flag for controlling write and read enable/disable of the communication buffer, where the initial state of the status flag is write-enabled and read-disabled. It is noted that upon write completion the status flag is set from read-disabled to read-enabled, and upon read completion the status flag is set from write-disabled to write-enabled (Column 2, lines 56-67). This is interpreted as write being disabled by a write completion notification, with the write processing not set to enabled until the read process is completed)****, wherein the end of the first symbol group duration coincides with a beginning of a second symbol group duration* ***(interpretation where write is disabled by a write completion notification, with the write processing not set to enabled until the read process is completed, also applies here)***," "*prior to an end of the second symbol group duration, disabling the processor upon completion of processing the second group of symbols…during a remainder of the second symbol group duration* ***(Column 2, lines 56-67)****, wherein the end of the second symbol group duration coincides with a beginning*

of a third symbol group duration ***(interpretation where write is disabled by a write completion notification, with the write processing not set to enabled until the read process is completed, also applies here)***," "*prior to an end of the third symbol group duration, disabling the processor upon completion of processing the third group of symbols…during a remainder of the third symbol group duration* ***(Column 2, lines 56-67)****, wherein the end of the third symbol group duration coincides with a beginning of a fourth symbol group duration* ***(interpretation where write is disabled by a write completion notification, with the write processing not set to enabled until the read process is completed, also applies here)***," "*prior to an end of the fourth symbol group duration, disabling the processor upon completion of processing the fourth group of symbols…during a remainder of the fourth symbol group duration* ***(Column 2, lines 56-67)****, wherein the end of the fourth symbol group duration coincides with a beginning of a fifth symbol group duration* ***(interpretation where write is disabled by a write completion notification, with the write processing not set to enabled until the read process is completed, also applies here)***," "*prior to an end of the fifth symbol group duration, disabling the processor upon completion of processing the fifth group of symbols…during a remainder of the fifth symbol group duration* ***(Column 2, lines 56-67)****, wherein the end of the fifth symbol group duration coincides with a beginning of a sixth symbol group duration* ***(interpretation where write is disabled by a write completion notification, with the write processing not set to enabled until the read process is completed, also applies here)***," and "*prior to an end of the sixth symbol group duration, disabling the processor upon completion of processing the sixth group*

of symbols…during a remainder of the sixth symbol group duration ***(Column 2, lines 56-67)***."

Horigan et al. discloses the idea of clock gating where an idle processor is disabled as disclosed in the limitation "*by gating off the processor clock, wherein the processor remains disabled* ***(Column 1, lines 40-43)***."

Sriram et al., et al., Tamura, Horigan et al., and Robertson et al. are analogous art in that they focus on the problem of buffering within a communication system.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the method of processing digital communication signals in a system including a plurality of buffers as disclosed by Sriram et al. with the idea of the using a five-entry buffer as disclosed by Robertson et al., which notes that it is prudent to include at least one more additional entry in several cases, notably where the receive clock is faster than the transmit clock and to account for maximum phase skew that may be present between transmit and receive clocks **(Page 9, paragraph 0077)**. Having five entries as opposed to three entries in a buffer not only can better account for the rate discrepancy between the system's receiver and a separate system's transmitter, but also can allow for more data to be stored before processing.

As for the idea of idea of processor/component disabling upon the completion of a task or process, Tamura notes instances of data being inaccessible if a particular process is still active **[Column 1, lines 51-58]**. Hence, it would be obvious for one skilled in the art to disable a processor once a task has been completed in order to allow further processing to occur.

As for Horigan et al., clock gating allows for the saving of power without impacting performance **[Column 1, lines 43-45]**.

As per **claim 19**, the combination of Sriram et al., Tamura, Horigan et al., and Robertson et al. discloses "*the method*" (*see rejection to* ***claim 18*** *above*). Sriram et al. further discloses "*each of the plurality of buffers holds a different number of digital samples* ***(despread symbols dumped into a finger symbol buffer)*** *based on communication conditions* ***(number of despread symbols dumped into a finger symbol buffer depends on the value of SF (symbol fingers); Page 3, paragraph 0041)***."

As per **claim 20**, the combination of Sriram et al., Tamura, Horigan et al., and Robertson et al. discloses "*the method*" (*see rejection to* ***claim 18*** *above*). Sriram et al. further discloses "*the communication conditions include multi-path delays* ***(system/method is capable of handling special cases of early/ontime/late correlations that occur when the on-time sample is near a chip boundary; Page 4, paragraph 0044; Figure 4a-4c)*** *and waveform features* ***(data portions are associated with time tracking of a particular symbol multipath; Page 2, paragraph 0033)***."

As per **claim 21**, the combination of Sriram et al., Tamura, Horigan et al., and Robertson et al. discloses "*the method*" (*see rejection to* ***claim 18*** *above*). Sriram et al. further discloses "*the paths are from a plurality of base stations* ***(the system is capable of performing CDMA base station operations (Page 4, paragraph 0048) in a multipath environment that may not be constant; Page 2, paragraph 0026)***."

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

9. As required by **M.P.E.P. 609(c)**, the applicant's submission of the Information Disclosure Statement dated July 23, 2009, and August 17, 2009, is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

CONCLUDING REMARKS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

10. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P 707.07(i):**

a(1). CLAIMS REJECTED IN THE APPLICATION

11. Per the instant office action, claims 1-4,6,7,9-15 and 17-22 have received a action on the merits and are subject of an action non-final.

12. The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line no(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HENRY YU whose telephone number is (571)272-9779. The examiner can normally be reached on Monday to Friday, 8:00 AM to 5:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TARIQ HAFIZ can be reached on (571) 272-6729. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/H. Y./
Examiner, Art Unit 2182
September 21, 2009

/Tariq Hafiz/
Supervisory Patent Examiner, Art Unit 2182